## GOVERNMENT COLLEGE OF ENGINEERING, JALGAON
**(An Autonomous Institute of Government of Maharashtra)**
National Highway No.6, JALGAON – 425 002

| | |
|---|---|
| Phone No.: 0257-2281522 | Fax No.: 0257-2281319 |
| Website : www.gcoej.ac.in | E-mail : princoej@redifmail.com |

Name of Examination : **Summer 2021** - (Preview)

Course Code & Course Name : **IN255U - Digital Circuits Design**

Generated At : **19-04-2022 14:58:58**

Maximum Marks : **60**          Duration : **3 Hrs**

Edit   Print   View Answer Key   Close   **Answer Key Submission Type:** Marking scheme with model answers and solutions of numerical

Instructions:

1. *All questions are compulsory.*
2. *Illustrate your answer with suitable figures/sketches wherever necessary.*
3. *Assume suitable additional data; if required.*
4. *Use of logarithmic table, drawing instruments and non programmable calculators is allowed.*
5. *Figures to the right indicate full marks.*

**1)**  **Solve Three questions**

a)  Write the advantages of digital system over Analog system  [6]

b)  Design and explain the X-OR gate and X-NOR gate using circuit and truth table  [6]

c)  State Demorgan's theorem .Prove the $x.y + y.z + x'.z = x.y + x'.z$ and design the digital circuit  [6]

**2)**  **Solve Three questions**

a)  Explain the 8421 BCD code ( Natural BCD code). Perform decimal additions and subtraction  using BCD  [6]

  i).  679.6 + 536.8

  ii).  38-15

b)  Design a digital system(logic gate circuit) for the following condition :  [6]
    The system output gets a logically zero signal if the 4-bit input number is multiple of 3; else output will be logically one status. Getting output from system only if the input binary number is greater than 2. (Design logical circuit)

c)  Design and explain  the full adder circuit with NAND gates with  truth table  [6]

**3)**  Solve any Two questions

a)  Explain n Bit Parallel Full Adder with block and circuit diagram  [6]

b)  Design and explain full adder using two 8 : 1 multiplexers with proper circuit diagram  [6]

c)  Realize a two input XOR gate by decoder and any other gates required (NAND gates are essential at the output of a decoder).  [6]

**4)**  **Solve any Two questions**

a)  Design mode 5 counter using JK flip-flops and implement it  [6]

b)  What is shift resister? Draw circuit diagram  for  [6]

  i).  Serial in /parallel out

  ii). Parallel in /serial out shift register using J-K flip-flops

c)  Explain with help of a diagram, the principle of operation of R-2R ladder D/A converter  [6]

**Auto Generated by SsOES v6.2**